CEG2400 - Microcomputer Systems

Lecture 13: Buses

Philip Leong

Slides: courtesy of John Lazzaro UCB

Introduction

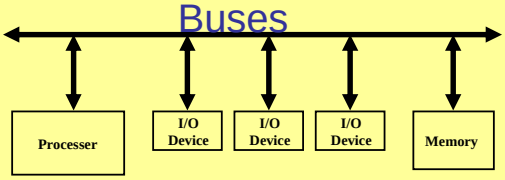
- Last week: discussed low level details of ARM memory bus
- This week, discuss buses in general along with the ARM AMBA bus

Buses

Shared physical wires that act to communicate signals between several devices (often "peripherals")

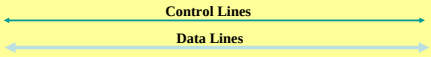
– Allow computers be expandable and customisable (more memory, better graphics card, webcam etc)

Recall: Disadvantage of Buses



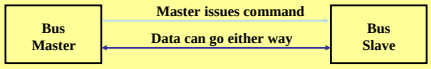
- It creates a communication bottleneck
  - The bandwidth of that bus can limit the maximum I/O throughput
- The maximum bus speed is largely limited by:
  - The length of the bus
  - The number of devices on the bus
  - The need to support a range of devices with:
    - Widely varying latencies
    - Widely varying data transfer rates

The General Organization of a Bus



- Control lines:
  - Signal requests and acknowledgments
  - Indicate what type of information is on the data lines
- Data lines carry information between the source and the destination:
  - Data and Addresses
  - Complex commands

Master versus Slave

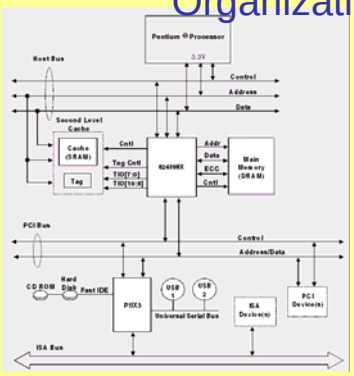


- A bus transaction includes two parts:
  - Issuing the command (and address) – request
  - Transferring the data – action
- Master is the one who starts the bus transaction by:
  - issuing the command (and address)
- Slave is the one who responds to the address by:
  - Sending data to the master if the master ask for data
  - Receiving data from the master if the master wants to send data

Types of Buses

- Processor-Memory Bus (design specific)
  - Short and high speed
  - Only need to match the memory system
    - Maximize memory-to-processor bandwidth
  - Connects directly to the processor
  - Optimized for cache block transfers
- I/O Bus (industry standard)
  - Usually is lengthy and slower
  - Need to match a wide range of I/O devices
  - Connects to the processor-memory bus or backplane bus
- Backplane Bus (standard or proprietary)
  - Backplane: an interconnection structure within the chassis
  - Allow processors, memory, and I/O devices to coexist
  - Cost advantage: one bus for all components

Example: Pentium System Organization

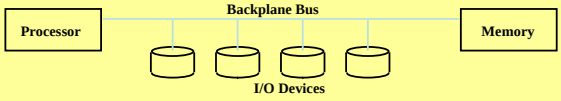


Processor/Memory Bus -- Design Specific

Backplane Bus – PCI
PCI Devices: Graphics
IO Control

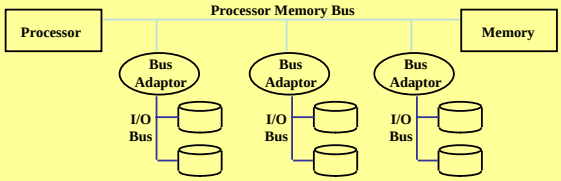
I/O Busses – IDE, USB & SCSI

System with One Bus: Backplane Bus



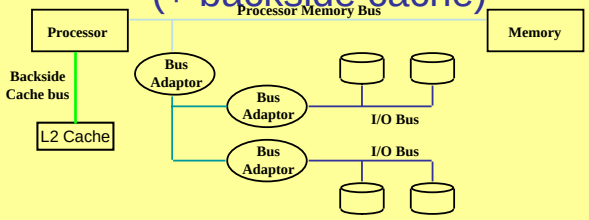
- A single bus (the backplane bus) is used for:
  - Processor to memory communication
  - Communication between I/O devices and memory
- Advantages: Simple and low cost
- Disadvantages: slow and the bus can become a major bottleneck
- Example: IBM PC - AT

A Two-Bus System



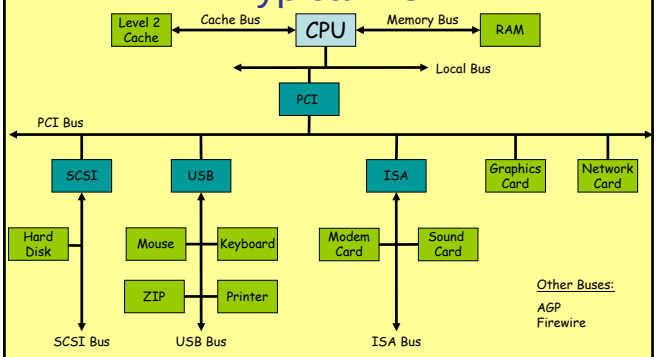
- I/O buses tap into the processor-memory bus via bus adaptors to speed match between bus types:
  - Processor-memory bus: mainly for processor-memory traffic
  - I/O buses: provide expansion slots for I/O devices
- Apple Macintosh-II
  - NuBus: Processor, memory, and a few selected I/O devices
  - SCSI Bus: the rest of the I/O devices

A Three-Bus System (+ backside cache)



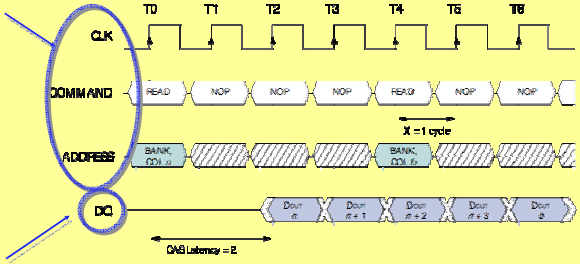
- A small number of backplane buses tap into the processor-memory bus
  - Processor-memory bus focus on traffic to/from memory
  - I/O buses are connected to the backplane bus
- Advantage: loading on the processor bus is greatly reduced & busses run at different speeds

Typical PC



Properties...

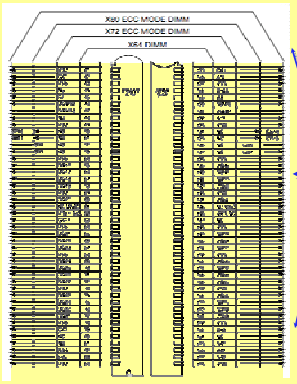
Control lines: Controls transactions, signals what is on data lines



Data lines: Carries information across the interface

Buses are an abstraction for communication: helps designers compose large, complex systems.

Buses defined in layers ...



Example: DIMM DRAM bus. The name of every wire is defined in a standards document.

- Transaction Protocols
- Signal Timing on Wires
- **Wires**
- Electrical Properties
- Mechanical Properties

JEDEC: Joint Electron Device Engineering Council. Makes the DRAM bus standards

Lower levels of DRAM bus

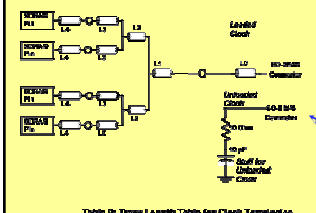


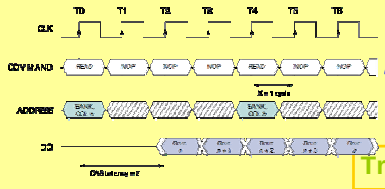
Table B: Trace Length Table for Clock Terminations

Segment	L0	L1	L2	L3	L4	Total Min	Total Max
Length	0.10"	1.00"	0.50"	0.50"	0.10"	2.40"	2.70"
Tolerance-Layer	±0.02" Outer	±0.02" Inner	±0.02" Inner	±0.02" Inner	±0.02" Outer		

- Transaction Protocols
- Signal Timing on Wires
- **Wires**
- Electrical Properties
- Mechanical Properties

Ideally, DIMMs made by any manufacturer should fit into any compliant socket, and work.

Upper levels of DRAM bus



TIMING PARAMETERS

SYMBOL*	-7E MIN	-7E MAX	-7S MIN	-7S MAX	UNITS
tAC (3)		5.4		5.4	ns
tAC (2)		5.4		6	ns
tAH	1.05		1.05		ns
tAS	1.5		1.5		ns
tCH	2.5		2.5		ns
tCL	2.5		2.5		ns
tCK (3)	7		7.5		ns
tCK (2)	7.5		10		ns
tCH-I	1.05		0.5		ns

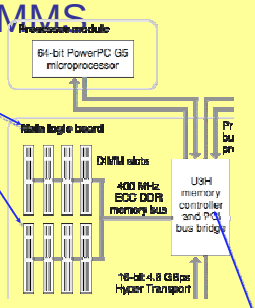
Collaboration between DRAM manufacturers (Samsung, Micron) and DRAM users (Intel, Cisco, ...).

- Transaction Protocols
- Signal Timing on Wires
- **Wires**
- Electrical Properties
- Mechanical Properties

Wires shared between many DIMMS

Apple Xserve G5 - has 8 DIMM slots, to support 8GB.

DIMMs respond to transaction requests. Since memory controller is only bus master, and there are a small number of DIMM slots, bus sharing is easy: **use dedicated wires to each slot.**

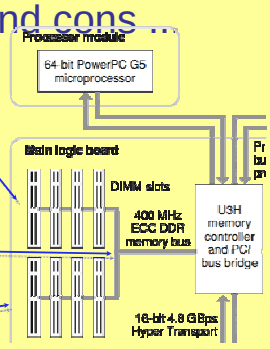


Memory controller is the only **"bus master"** - it can **start transactions** on the bus, but the DIMMs cannot.

Buses: pros and cons ...

+++ Low cost. One set of wires from memory controller can support up to 8 DIMMs.

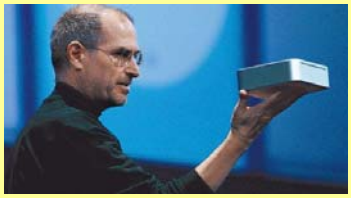
--- Latency of bus increases with length of wires (needed to reach all 8 DIMM sockets), and the loading of 8 DIMMs. Must design for worst-case (8 DIMMs), even if only 1 DIMM is present.



--- Shared wires limit maximum bandwidth from memory. If memory controller had 8 sets of dedicated wires, one per DIMM, memory bandwidth would be much better (but more expensive).

Buses turn a CPU into a product

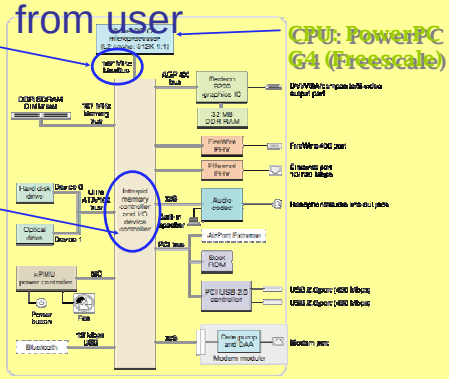
Case Study: Mac Mini



Many other buses hidden from user

Processor bus – how the CPU talks to all the other peripherals. Not standardised.

Bus controller – just 1 for low cost. High end products have 2 (fast North bridge, slow South bridge)



Constraints: Size, low price

Size fixed by form factor (physical size) of desktop DIMMs. Laptop DRAM is smaller but too expensive for a $499 product.

Uses many standard parallel buses …

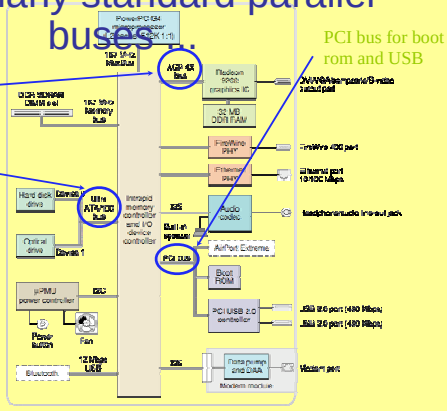
AGP 4X bus (graphics chip)

ATA/100 bus (hard disk, DVD/CDROM)

PCI, ATA, AGP devices can be bus master for DMA

Disk can directly write to RAM

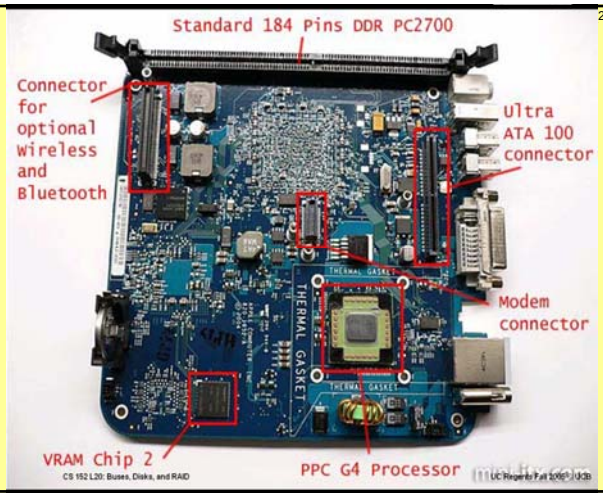
PCI bus for boot rom and USB

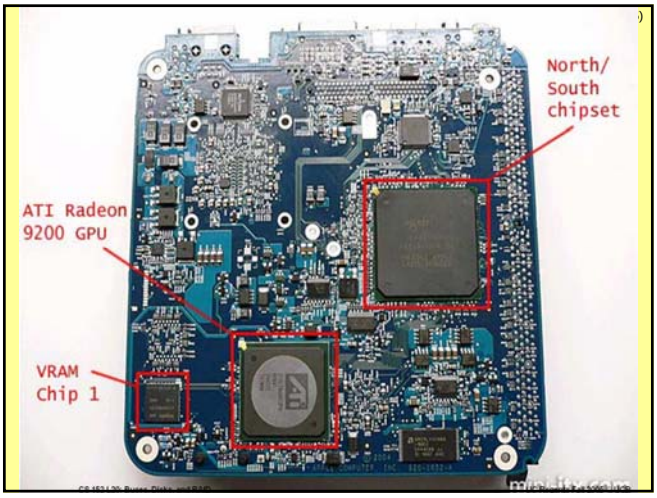


Users expansion via serial buses

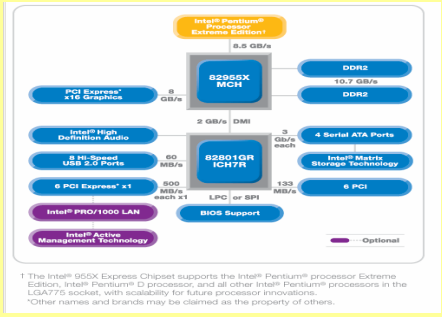
- Serial – data sent over one wire, bit-by-bit
- Advantages
  - low skew (problems due to signal travelling at different rates across parallel wires)
  - Small number of wires so lower cost for cables and connectors
- Disadvantages
  - Less parallel wires so possibly lower bandwidth if skew is not the major bottleneck

USB, FireWire Ethernet.



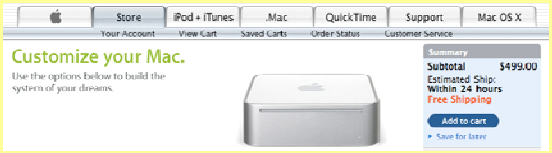


CPU & Device Speeds



Cost

- Parts cost $274.69
- Parts + manufacturing $283.37
- Source iSuppli Corp

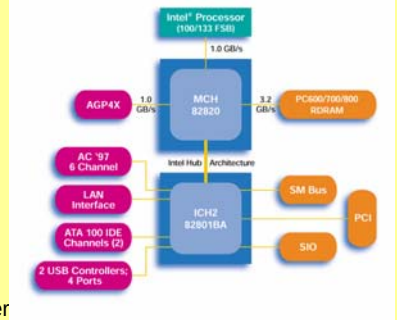


Summary: What defines a bus?

- **Transaction Protocol**
- **Timing and Signaling Specification**
- Bunch of Wires
- **Electrical Specification**
- **Physical / Mechanical Characteristics – the connectors**

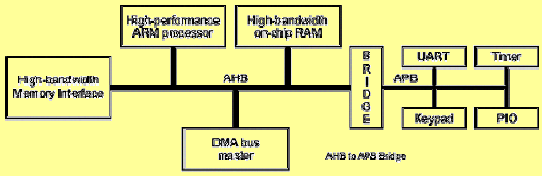
Main components of Intel Chipset: Pentium II/III

- Northbridge:
  - Handles memory
  - Graphics
- Southbridge: I/O
  - PCI bus
  - Disk controllers
  - USB controllers
  - Audio (AC97)
  - Serial I/O
  - Interrupt controller
  - Timers



AMBA - 1

- Advanced Microcontroller Bus Architecture
  - Standard of on-chip communication between different macrocells for high performance embedded system design
  - Hierarchical Bus architecture



AMBA - 2

- AMBA buses
  - AHB (Advanced High Performance Bus)
    - Connect between high-performance system modules
  - ASB (Advanced System Bus)
    - Subset of AHB
  - APB (Advanced Peripheral Bus)
    - Simple interface for low-performance peripherals

AMBA - 3

- AMBA buses (cont'd)

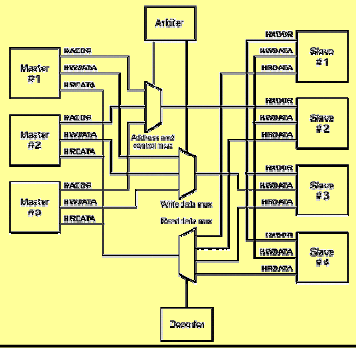
AHB	ASB	APB
- burst transfers - split transactions - single-cycle bus master handover - single-clock edge operation - wider data bus configurations (64/128 bits) - multiple bus masters (up to 16) - pipelined operation	- burst transfers - pipelined operation - multiple bus masters	- low power - latched address and control - simple interface - suitable for many peripherals

AMBA - 4

- AMBA AHB component
  - Master
    - Initiate read and write operations by providing an address and control information. Only one bus master is allowed to actively use the bus at any one time.
  - Slave
    - Responds to a read or write operation within a given address-space range. The bus slave signals back to the active master the success, failure or waiting of the data transfer.
  - Arbiter
    - Ensures that only one bus master at a time is allowed to initiate data transfers. Can use the priority
  - Decoder
    - Decode the address of each transfer and provide a select signal for the slave that is involved in the transfer.

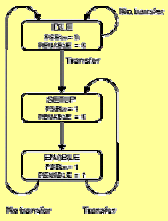
AMBA - 5

- AMBA AHB component (cont'd)



AMBA - 6

- AMBA APB
  - APB bridge: only master in APB. Act as slave in AHB
  - APB slave: peripherals
  - Simple protocol



- Processor core
  - Master in AHB
  - Connect through the memory interface of core